WHAT IS CLAIMED IS:

1. A key switch signal recognition circuit comprising:
a plurality of key switch buttons, said key switch buttons each provided with an electrically conductive element;
a plurality of key switch key signal output lines; and
a plurality of contact areas arranged on a substrate corresponding to said key switch buttons, said contact areas each comprising a first wire set and a second wire set, said first wire set comprising at least one wire having one end connected to a common line and an opposite end forming an open end, said second wire set comprising at least one wire respectively disposed in parallel to and electrically insulated from the wire of said first wire set, the wire of said second wire set being respectively connected to the key switch signal output line which is selected subject to a predetermined bit encoding mode;
when one of said key switch buttons is depressed to touch the corresponding contact area, the electrically conductive element of the depressed key switch button electrically connects the first wire set and second wire set of the touched contact area, causing the respective key switch signal output line to send a key switch signal corresponding to the depressed key switch button.
2. The key switch signal recognition circuit of claim 1, wherein said bit encoding mode is a BCD encoding format.
3. The key switch signal recognition circuit of claim 1, wherein said key switch signal output lines comprises a grounding wire.
4. The key switch signal recognition circuit of claim 1, wherein the open end of the wire of the first wire set and the second wire set is terminated into two parallel end portions.
5. The key switch signal recognition circuit of claim 1, wherein the key switch signal output lines are respectively connected to a signal input end of a respective AND gate, which outputs a triggering signal through an output end thereof when the key switch signal output line of the corresponding contact area is logically high.

6. The key switch signal recognition circuit of claim 1, wherein the key switch signal output lines are further respectively connected to a debouncing circuit.